



Description

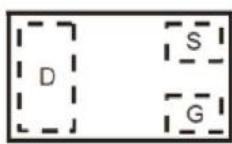
JMT N-channel Enhancement Mode Power MOSFET

Features

- 20V, 0.75A
- $R_{DS(ON)} < 165\text{m}\Omega$ @ $V_{GS} = 4.5\text{V}$
- $R_{DS(ON)} < 260\text{m}\Omega$ @ $V_{GS} = 2.5\text{V}$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired
- ESD Protected: 2KV

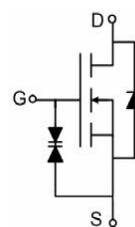
Application

- Load Switch
- PWM Application
- Power management



DFN1006-3L top view

Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
34K	JMTD3134K	TAPING	DFN1006-3L	7inch	10000	400000

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		± 10	V
I_D	Continuous Drain Current		$T_A = 25^\circ\text{C}$	A
			$T_A = 100^\circ\text{C}$	A
I_{DM}	Pulsed Drain Current ^{note1}		3	A
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	0.15	W
$R_{\theta JA}$	Thermal Resistance, Junction to Case		833	°C/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C

**Electrical Characteristics** ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	20	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}}=20\text{V}$, $V_{\text{GS}}=0\text{V}$,	-	-	1	μA
I_{GSS}	Gate to Body Leakage Current	$V_{\text{DS}}=0\text{V}$, $V_{\text{GS}}= \pm 10\text{V}$	-	-	± 10	μA
On Characteristics						
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}$, $I_D=250\mu\text{A}$	0.4	0.7	1.0	V
$R_{\text{DS}(\text{on})}$ note2	Static Drain-Source on-Resistance	$V_{\text{GS}}=4.5\text{V}$, $I_D=0.5\text{A}$	-	125	240	$\text{m}\Omega$
		$V_{\text{GS}}=2.5\text{V}$, $I_D=0.4\text{A}$	-	185	280	
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{\text{DS}}=10\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1.0\text{MHz}$	-	60	-	pF
C_{oss}	Output Capacitance		-	22	-	pF
C_{rss}	Reverse Transfer Capacitance		-	12	-	pF
Q_g	Total Gate Charge	$V_{\text{DS}}=10\text{V}$, $I_D=0.75\text{A}$, $V_{\text{GS}}=4.5\text{V}$	-	1	-	nC
Q_{gs}	Gate-Source Charge		-	0.28	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	0.22	-	nC
Switching Characteristics						
$t_{\text{d}(\text{on})}$	Turn-on Delay Time	$V_{\text{DS}}=10\text{V}$, $I_D=0.5\text{A}$, $R_{\text{GEN}}=10\Omega$, $V_{\text{GS}}=4.5\text{V}$	-	2	-	ns
t_r	Turn-on Rise Time		-	19	-	ns
$t_{\text{d}(\text{off})}$	Turn-off Delay Time		-	10	-	ns
t_f	Turn-off Fall Time		-	23	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward Current	-	-	0.75	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	3	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{\text{GS}}=0\text{V}$, $I_s=0.75\text{A}$	-	-	1.2	V

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$

Typical Performance Characteristics

Figure 1: Output Characteristics

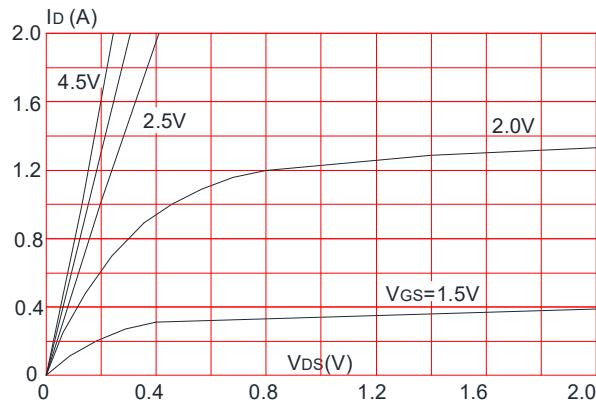


Figure 3: On-resistance vs. Drain Current

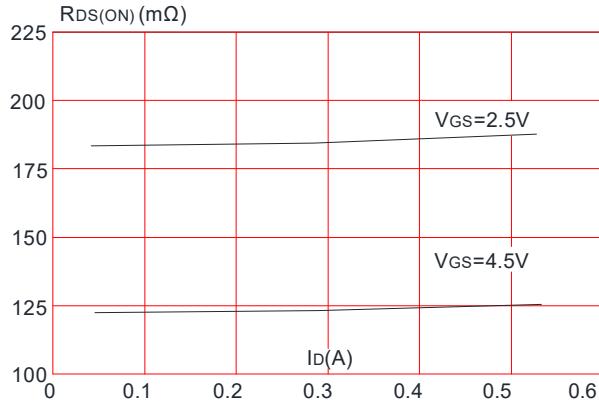


Figure 5: Gate Charge Characteristics

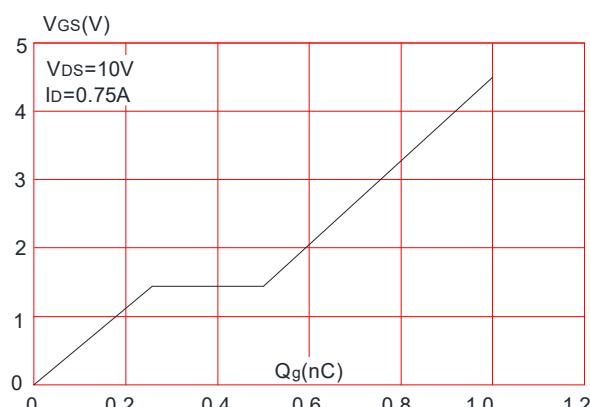


Figure 2: Typical Transfer Characteristics

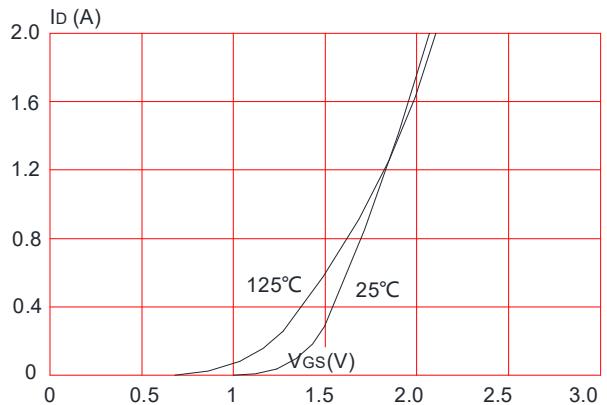


Figure 4: Body Diode Characteristics

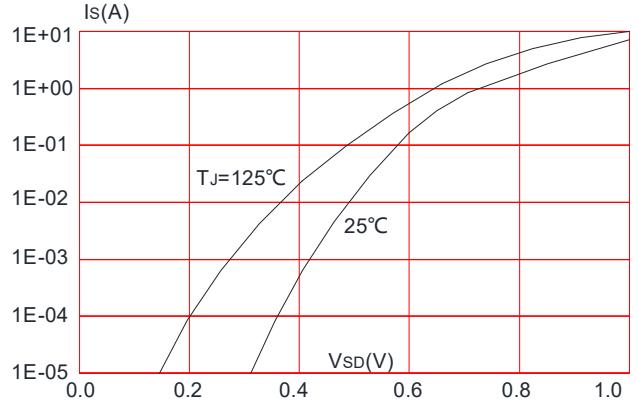


Figure 6: Capacitance Characteristics

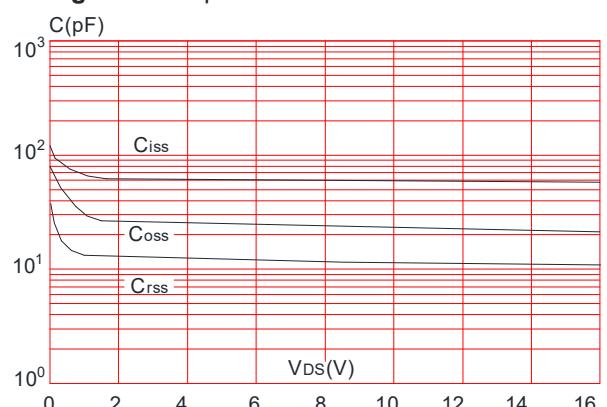


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

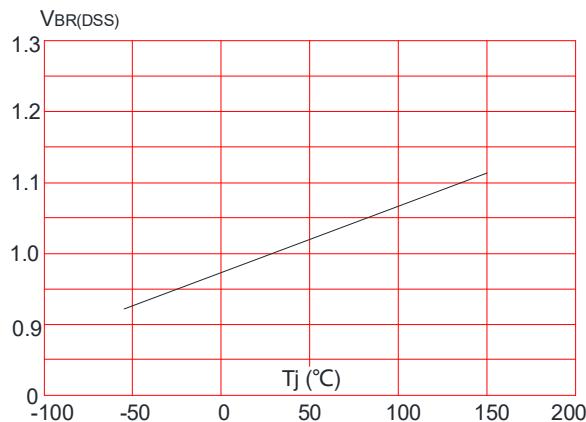


Figure 8: Normalized on Resistance vs. Junction Temperature

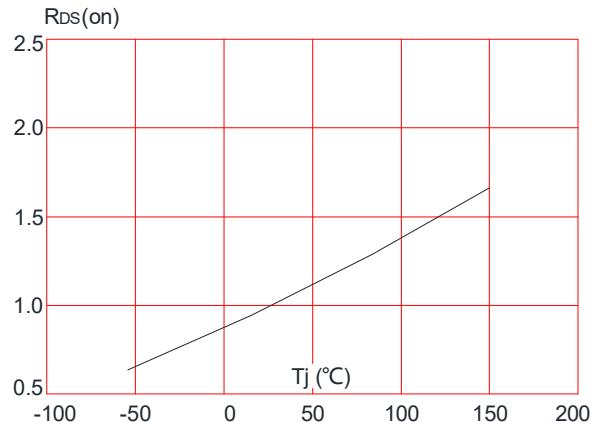


Figure 9: Maximum Safe Operating Area

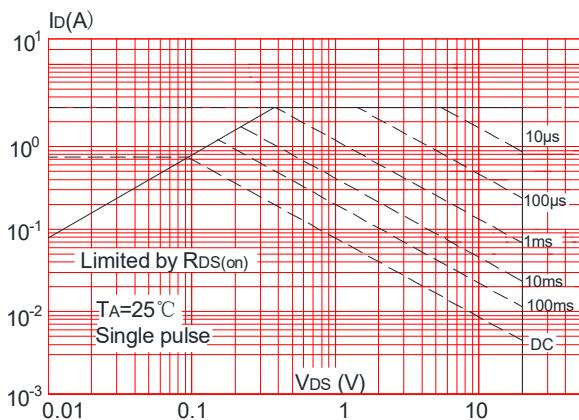


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

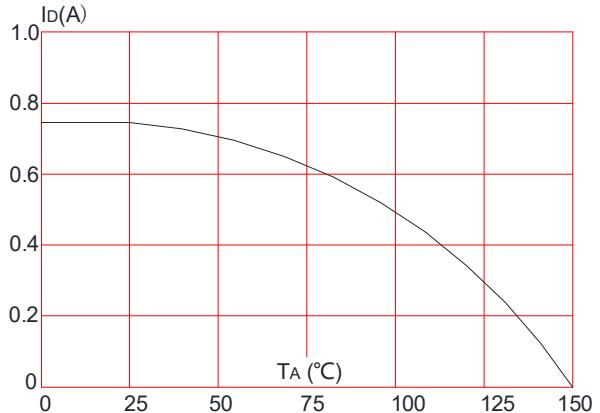
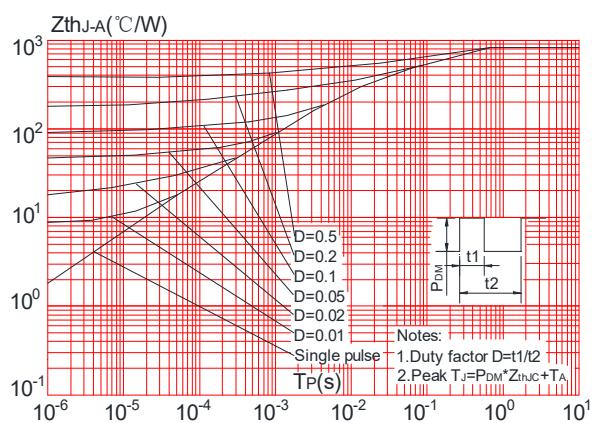


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



Test Circuit

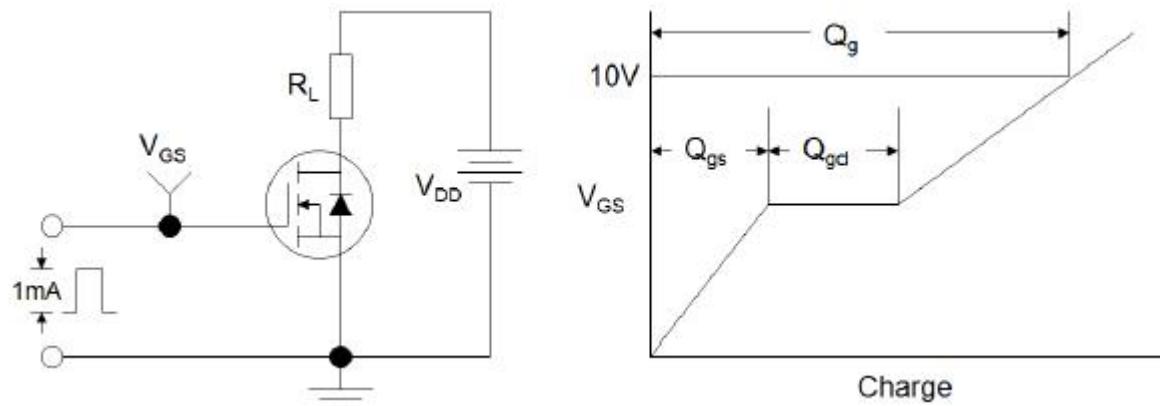


Figure1:Gate Charge Test Circuit & Waveform

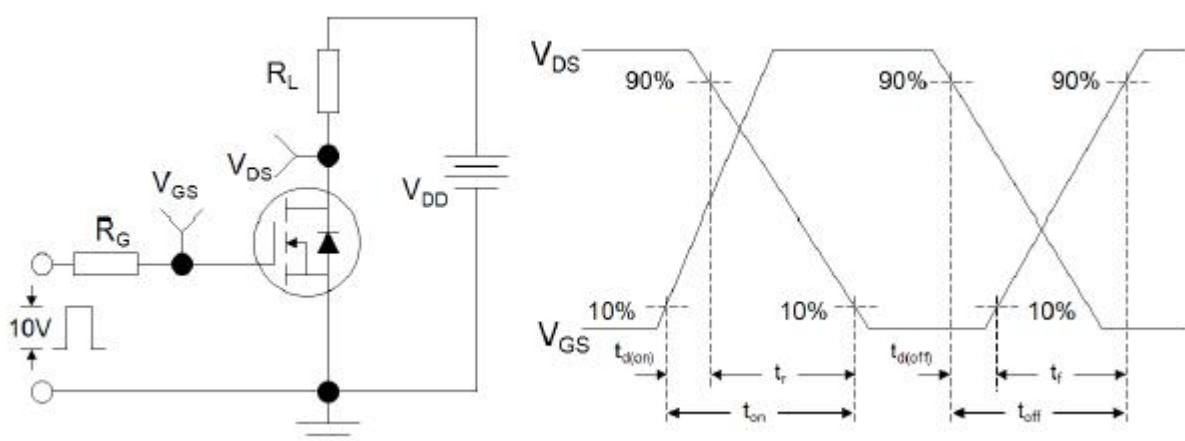


Figure 2: Resistive Switching Test Circuit & Waveforms

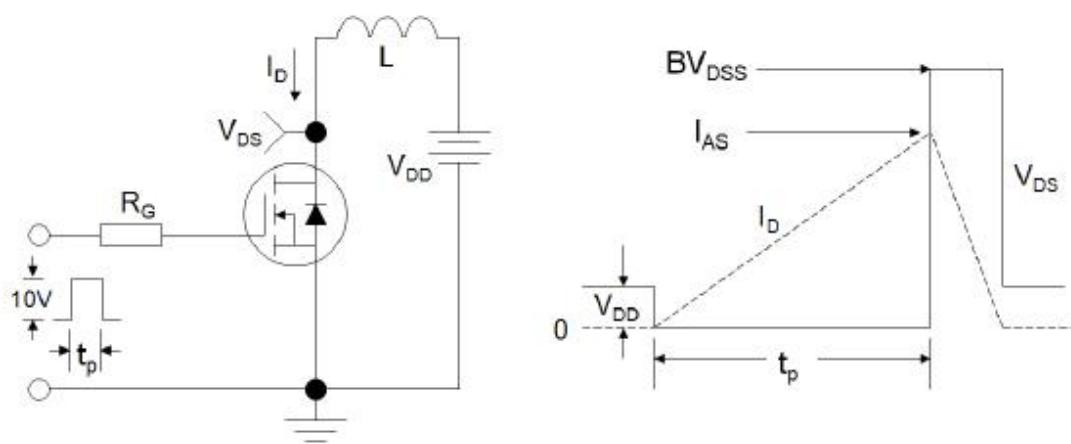
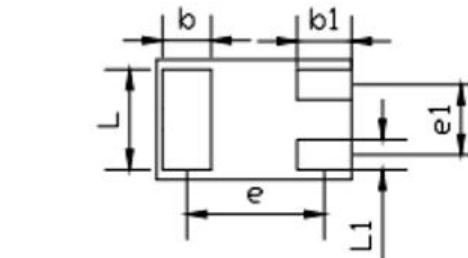
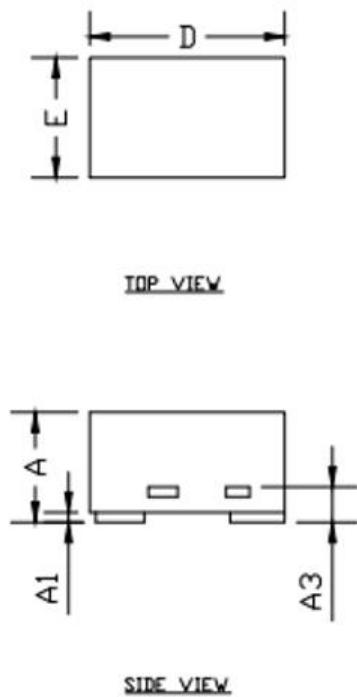


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



Package Mechanical Data-DFN1006-3L



PKG	COMMON DIMENSION (MM)			
	REF.	MIN.	NOM.	MAX
DFN1006				
A	REF.	>0.4	-	0.50
A1		0.00	-	0.05
A3		0.127	REF.	
D		0.95	1.00	1.05
E		0.55	0.60	0.65
b		0.20	0.25	0.30
b1		0.20	0.30	0.40
L		0.45	0.50	0.55
L1		0.10	0.15	0.20
e			0.675	
e1			0.35	

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